REMARKS

An inadvertent error was made by not marking for deletion a section from claim 18 and not correcting a word to its singular form. It appears that the Examiner may have recognized this error. For the sake of clarity, a replacement set of claims is included, and claim 18 is amended to reflect its desired form.

If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Stephen M. De Klerk at (408) 720-8300.

Please charge any shortages and credit any overages to Deposit Account No. 02-2666. Any necessary extension of time for response not already requested is hereby requested. Please charge any corresponding fee to Deposit Account No. 02-2666.

Respectfully submitted,

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IN THE CLAIMS

Please amend claim 18 of the following claims which are pending in the present application, as shown:

1-16. (Cancelled)

17. (Previously presented) A semiconductor package, comprising:

a substrate that includes a top surface and an exposed external opposite surface including a first, inner region, a second, outer region around the inner region, and a third region that separates the first and second regions; and

a plurality of contacts including a first plurality of contacts and a second plurality of contacts, said first plurality of contacts located in a four-by-four matrix in the first region, and said second plurality of contacts located in the second region such that a smallest distance between adjacent contacts in both the first and second regions are smaller than a distance between the first and second regions, wherein the third region does not have any contacts located therein.

18. (Currently amended) The semiconductor package of claim 17, wherein the smallest distance between adjacent contacts in the first region ~~are~~ is equal to the smallest distance between adjacent contacts in the second region ~~is smaller than the distance between the first and second regions~~.

19-20. (Cancelled)

21. (Previously presented) The semiconductor package of claim 17, wherein the plurality of contacts comprises a plurality of contact pads.

22. (Previously presented) The semiconductor package of claim 21 further comprising a plurality of solder balls attached to said contact pads of said first and second plurality of contacts.

23. (Previously presented) The semiconductor package of claim 17 wherein each of the second plurality of contacts is contained within a dimensional profile of an integrated circuit coupled to the top surface of the substrate.

24. (Cancelled)

25. (Previously presented) The semiconductor package of claim 17 wherein said top surface of said substrate has a plurality of bond pads.

26. (Previously presented) The semiconductor package of claim 25 wherein said top surface of said substrate has a ground bus that is connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

27. (Previously presented) The semiconductor package of claim 17 wherein said first plurality of contacts comprises at least five rows of contacts.

28. (Previously presented) The semiconductor package of claim 25 wherein said top surface of said substrate has a power bus that is connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

29. (Cancelled)

30. (Previously presented) A semiconductor package, comprising:

a substrate that includes a top surface having a plurality of bond pads, and an exposed external opposite surface including an inner region, an outer region, and a middle region that separates the inner and outer regions;

a plurality of contacts including a first plurality of contacts and a second plurality of contacts, said first plurality of contacts located in the outer region, and said second plurality of contacts located in the inner region such that the smallest distances between adjacent contacts in the inner and outer regions are smaller than a distance between the inner and outer regions, wherein the middle region is free of contacts; and

an integrated circuit that is mounted to said top surface of said substrate and electrically coupled to said plurality of bond pads, wherein said first and

second plurality of contacts are located respectively outside and inside a dimensional profile of said integrated circuit.

31. (Previously presented) The semiconductor package of claim 30, wherein the distances between adjacent contacts in the inner region are equal to the distances between adjacent contacts in the outer region.

32-33. (Cancelled)

34. (Previously presented) The semiconductor package of claim 30 further comprising a plurality of electrically conductive members attached to said plurality of contacts of said first and second plurality of contacts.

35. (Previously presented) The semiconductor package of claim 30 wherein said top surface of said substrate has a ground bus that is coupled to said integrated circuit and connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

36. (Previously presented) The semiconductor package of claim 30 wherein said top surface of said substrate has a power bus that is coupled to said integrated circuit and connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

37. (Previously presented) The semiconductor package of claim 30 further comprising an encapsulant enclosing said integrated circuit.

38-39. (Cancelled)

40. (Previously presented) An integrated circuit package for an integrated circuit which has a dimensional profile, comprising:

a substrate that includes a top surface, and an exposed external opposite surface defined by a first region that is substantially equal to the dimensional profile of the integrated circuit, a second region, and a third region that separates the first and second regions; and

a plurality of contacts including a first plurality of contacts and a second plurality of contacts, said first plurality of contacts located within the second region, and said second plurality of contacts located in the first region such that a first smallest distance between adjacent contacts in the first region is smaller than a second smallest distance between the first and second regions, said third region being a contact free region.

41. (Previously presented) The integrated circuit package of claim 40, wherein a distance between adjacent contacts in first region is the same as the distance between adjacent contacts in the second region.

42. (Previously presented) The integrated circuit package of claim 40 further comprising a plurality of solder balls attached to said plurality of contacts.

43. (Previously presented) The integrated circuit package of claim 40 wherein said top surface of said substrate has a ground bus that is connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

44. (Previously presented) The integrated circuit package of claim 40 wherein said top surface of said substrate has a power bus that is connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

45. (Previously presented) A semiconductor package, comprising:

a substrate which has a top surface and an exposed external bottom surface, said external bottom surface having a plurality of contact pads, said plurality of contact pads consisting only of:

an outer array of contact pads, each of said contact pads separated from each other by a first distance;

a center array of contact pads, arranged in a four-by-four array, each of said contact pads separated by a second distance, said center array of contact pads

being separated from said outer array of contact pads by a third distance which is larger than said first and second distances; and

a plurality of conductive contacts attached to said contact pads of said substrate.

46. (Previously presented) The semiconductor package of claim 45 wherein said outer array of contact pads is located outside an outer dimensional profile of an integrated circuit coupled to the top surface of said substrate.

47. (Previously presented) The semiconductor package of claim 45 wherein said center array of contact pads is located inside the outer dimensional profile of an integrated circuit coupled to the top surface of said substrate.

48. (Previously presented) The semiconductor package of claim 45 wherein said outer array of contact pads is located outside an outer dimensional profile of an integrated circuit coupled to the top surface of said substrate, and wherein said center array of contact pads is located inside the outer dimensional profile of said integrated circuit.

49. (Previously presented) The semiconductor package of claim 45 wherein a distance between adjacent contact pads in said outer array is the same as the distance between adjacent contact pads in said center array.

50. (Previously presented) The semiconductor package of claim 45 wherein the smallest distance between adjacent contact pads in the outer array is smaller than the distance between the outer array of contact pads and the center array of contact pads.

51. (Previously presented) The semiconductor package of claim 45 wherein the top surface of said substrate has a ground bus that is connected to said center array of contact pads by a plurality of vias that extend through said substrate.

52. (Previously presented) The semiconductor package of claim 45 wherein the conductive contacts are solder balls.

53. (Previously presented) A semiconductor package, comprising:

a substrate that includes a top surface having a bus and an exposed external opposite surface including a first, inner region, a second, outer region around the inner region, and a third region that separates the first and second regions;

a plurality of contacts including a first plurality of contacts and a second plurality of contacts, said first plurality of contacts located in a four-by-four matrix in the first region, and said second plurality of contacts located in the second region such that a smallest distance between adjacent contacts in both the

first and second regions are smaller than a distance between the first and second regions, wherein the third region does not have any contacts located therein; and

a plurality of via interconnecting the first bus with a plurality of the first contacts.

54. (Previously presented) The semiconductor package of claim 53 wherein the top surface has a second bus, further comprising a plurality of vias interconnecting the second bus with a plurality of the second contacts.